WHAT IS CLAIMED IS:

1.   1.   A read channel, comprising:

2   an equalizer configured to equalize a digital signal to provide equalized

3   reproduced signals; and

4   a Viterbi detector capable of receiving the equalized reproduced signals and

5   converting the reproduced signals into a digital output signal indicative of data stored on

6   a recording medium;

7   wherein the equalizer is implemented using a coefficient learning circuit that

8   adaptively updates coefficients for the equalizer based upon a cosine function.

1   2.   The read channel of claim 1, wherein the coefficient learning circuit

2   adjusts coefficients using a tap coefficient update equation having a first parameter, k, for

3   modifying a magnitude response.

1   3.   The read channel of claim 2, wherein the first parameter, k, is adjusted

2   according to $k=k-g*(f(a_{k+1})+f(a_{k-1}))*e_k$, where k is the cosine equalizer parameter for

3   modifying the magnitude response, g is an update attenuation gain, and e_k is an error

4   signal based on a difference between a noisy equalized signal and a desired noiseless

5   signal.

1   4.   The read channel of claim 2, wherein the coefficient learning circuit

2   adjusts coefficients using a tap coefficient update equation having a second parameter, j,

3   for modifying a phase response.

1   5.   The read channel of claim 4, wherein the second parameter, j, is adjusted

2   according to $j=j-g*(f(a_{k+2})+f(a_{k-2}))*e_k$, where j is the cosine equalizer parameter for

3   modifying the phase response, g is an update attenuation gain, and e_k is an error signal

4   based on a difference between a noisy equalized signal and a desired noiseless signal.

1   6.   The read channel of claim 1, wherein the coefficient learning circuit

2   adjusts coefficients using a tap coefficient update equation having a parameter, j, for

3   modifying a phase response.

1   7.   The read channel of claim 1, wherein the coefficient learning circuit

2   adjusts coefficients, w_i, according to $w_i=w_i-g*f(a_{k-i})*e_k$, where g is a provided update

3   attenuation gain and $f(a_{k-i})$ is based on the cosine function.

1   8.   The read channel of claim 7, wherein $f(a_{k-i})$ is chosen to be $a_{k-i}-a_{k-i-2}$,

2   wherein written bits that are to be detected, a_{k-i} , are convolved with a PR4 response

3   based upon the cosine function.

1   9.   The read channel of claim 7, wherein $f(a_{k-i})$ is chosen to be

2       $a_{k-i} + a_{k-i-1} - a_{k-i-2} - a_{k-i-3}$, wherein written bits that are to be detected, a_{k-i} , are convolved

3   with the EPR4 response based upon the cosine function.

1   10.   The read channel of claim 7, wherein $f(a_{k-i})$ is chosen to be $a_{k-i}t_k$, wherein

2   written bits that are to be detected, a_{k-i} , are convolved with t_k based upon the cosine

3   function.

1   11.   The read channel of claim 7, wherein $f(a_{k-i})$ is chosen to be $a_{k-i}h_k$, wherein

2   written bits that are to be detected, a_{k-i} , are convolved with h_k based upon the cosine

3   function.

1   12.   A waveform equalizer that equalizes a waveform of a reproduction signal

2   obtained by reproducing marks and non-marks recorded on a recording medium,

3   comprising:

4   a delay element that delays a propagation of the reproduced signal;

5   a plurality of multipliers that multiply predetermined coefficients by the

6   reproduction signal and the delayed signal from the delay element;

7   a coefficient learning circuit that adaptively updates the predetermined

8   coefficients for each of the plurality of multipliers; and

9   an adder that adds outputs from the plurality of multipliers;

10   wherein the coefficient learning circuit adaptively updates coefficients for the

11   equalizer based upon a cosine function.

1   13.   The waveform equalizer of claim 12, wherein the coefficient learning

2   circuit adjusts coefficients using a tap coefficient update equation having a first

3   parameter, k, for modifying a magnitude response.

1   14.   The waveform equalizer of claim 13, wherein the first parameter, k, is

2   adjusted according to $k=k-g*(f(a_{k+1})+f(a_{k-1}))*e_k$, where k is the cosine equalizer

3   parameter for modifying the magnitude response, g is an update attenuation gain, and e_k

4   is an error signal based on a difference between a noisy equalized signal and a desired

5   noiseless signal.

1   15.   The waveform equalizer of claim 13, wherein the coefficient learning

2   circuit adjusts coefficients using a tap coefficient update equation having a second

3   parameter, j, for modifying a phase response.

1   16.   The waveform equalizer of claim 15, wherein the second parameter, j, is

2   adjusted according to $j=j-g*(f(a_{k+2})+f(a_{k-2}))*e_k$, where j is the cosine equalizer parameter

3   for modifying the phase response, g is an update attenuation gain, and e_k is an error signal

4   based on a difference between a noisy equalized signal and a desired noiseless signal.

1   17.   The waveform equalizer of claim 12, wherein the coefficient learning

2   circuit adjusts coefficients using a tap coefficient update equation having a parameter, j,

3   for modifying a phase response.

1   18.   The waveform equalizer of claim 12, wherein the coefficient learning

2   circuit adjusts coefficients, w_i, according to $w_i=w_i-g*f(a_{k-i})*e_k$, where g is a provided

3   update attenuation gain and $f(a_{k-i})$ is based on the cosine function.

1   19.   The waveform equalizer of claim 18, wherein $f(a_{k-i})$ is chosen to be $a_{k-i}-a_{k-i-2}$,

2   wherein written bits that are to be detected, a_{k-i} , are convolved with a PR4 response

3   based upon the cosine function.

1   20.   The waveform equalizer of claim 18, wherein $f(a_{k-i})$ is chosen to be

2    $a_{k-i} + a_{k-i-1} - a_{k-i-2} - a_{k-i-3}$, wherein written bits that are to be detected, a_{k-i} , are convolved

3   with the EPR4 response based upon the cosine function.

1   21.   The waveform equalizer of claim 18, wherein $f(a_{k-i})$ is chosen to be $a_{k-i}t_k$,

2   wherein written bits that are to be detected, a_{k-i} , are convolved with t_k based upon the

3   cosine function.

1   22.   The waveform equalizer of claim 18, wherein $f(a_{k-i})$ is chosen to be $a_{k-i}h_k$,

2   wherein written bits that are to be detected, a_{k-i} , are convolved with h_k based upon the

3   cosine function.

1   23.   A signal processing system, comprising:

2   memory for storing data therein; and

3   a processor, coupled to the memory, for equalizing a digital signal to provide

4   equalized reproduced signals, the processor adaptively updates coefficients for the

5   equalizer based upon a cosine function.

1   24.   The signal processing system of claim 23, wherein the processor adjusts

2   coefficients using a tap coefficient update equation having a first parameter, k, for

3   modifying a magnitude response.

1   25.   The signal processing system of claim 24, wherein the first parameter, k,

2   is adjusted according to $k=k-g*(f(a_{k+1})+f(a_{k-1}))*e_k$, where k is the cosine equalizer

3   parameter for modifying the magnitude response, g is an update attenuation gain, and e_k

4   is an error signal based on a difference between a noisy equalized signal and a desired

5   noiseless signal.

1   26.   The signal processing system of claim 24, wherein the processor adjusts

2   coefficients using a tap coefficient update equation having a second parameter, j, for

3   modifying a phase response.

1   27.   The signal processing system of claim 26, wherein the second parameter,

2   j, is adjusted according to $j=j-g*(f(a_{k+2})+f(a_{k-2}))*e_k$, where j is the cosine equalizer

3   parameter for modifying the phase response, g is an update attenuation gain, and e_k is an

4   error signal based on a difference between a noisy equalized signal and a desired

5   noiseless signal.

1   28.   The signal processing system of claim 23, wherein the processor adjusts

2   coefficients using a tap coefficient update equation having a parameter, j, for modifying a

3   phase response.

1   29.   The signal processing system of claim 23, wherein the coefficient learning

2   circuit adjusts coefficients, w_i, according to $w_i = w_i - g * f(a_{k-i}) * e_k$, where g is a provided

3   update attenuation gain and $f(a_{k-i})$ is based on the cosine function.

1   30.   The signal processing system of claim 29, wherein $f(a_{k-i})$ is chosen to be

2    $a_{k-i} - a_{k-i-2}$, wherein written bits that are to be detected, a_{k-i}, are convolved with a PR4

3   response based upon the cosine function.

1   31.   The signal processing system of claim 29, wherein $f(a_{k-i})$ is chosen to be

2    $a_{k-i} + a_{k-i-1} - a_{k-i-2} - a_{k-i-3}$, wherein written bits that are to be detected, a_{k-i}, are convolved

3   with the EPR4 response based upon the cosine function.

1   32.   The signal processing system of claim 29, wherein $f(a_{k-i})$ is chosen to be

2    $a_{k-i} t_k$, wherein written bits that are to be detected, a_{k-i}, are convolved with t_k based upon

3   the cosine function.

1   33.   The signal processing system of claim 29, wherein $f(a_{k-i})$ is chosen to be

2    $a_{k-i} h_k$, wherein written bits that are to be detected, a_{k-i}, are convolved with h_k based upon

3   the cosine function.

1   34.   A magnetic storage device, comprising:

2   a magnetic storage medium for recording data thereon;

3   a motor for moving the magnetic storage medium;

4   a head for reading and writing data on the magnetic storage medium;

5   an actuator for positioning the head relative to the magnetic storage medium; and

6   a data channel for processing encoded signals on the magnetic storage medium,

7   the data channel comprising an equalizer configured to equalize a digital signal to

8   provide equalized reproduced signals and a Viterbi detector capable of receiving the

9   equalized reproduced signals and converting the reproduced signals into a digital output

10   signal indicative of data stored on a recording medium; wherein the equalizer is

11   implemented using a coefficient learning circuit that adaptively updates coefficients for

12   the equalizer based upon a cosine function.

1   35.   The magnetic storage device of claim 34, wherein the equalizer adjusts

2   coefficients using a tap coefficient update equation having a first parameter, k, for

3   modifying a magnitude response.

1   36.   The magnetic storage device of claim 35, wherein the first parameter, k, is

2   adjusted according to $k=k-g*(f(a_{k+1})+f(a_{k-1}))*e_k$, where k is the cosine equalizer

3   parameter for modifying the magnitude response, g is an update attenuation gain, and e_k

4   is an error signal based on a difference between a noisy equalized signal and a desired

5   noiseless signal.

1   37.   The magnetic storage device of claim 35, wherein the equalizer adjusts

2   coefficients using a tap coefficient update equation having a second parameter, j, for

3   modifying a phase response.

1   38.   The magnetic storage device of claim 37, wherein the second parameter, j,

2   is adjusted according to $j=j-g*(f(a_{k+2})+f(a_{k-2}))*e_k$, where j is the cosine equalizer

3   parameter for modifying the phase response, g is an update attenuation gain, and e_k is an

4   error signal based on a difference between a noisy equalized signal and a desired

5   noiseless signal.

1   39.   The magnetic storage device of claim 34, wherein the equalizer adjusts

2   coefficients using a tap coefficient update equation having a parameter, j, for modifying a

3   phase response.

1   40.   The magnetic storage device of claim 34, wherein the coefficient learning

2   circuit adjusts coefficients, w_i, according to $w_i=w_i-g*f(a_{k-i})*e_k$, where g is a provided

3   update attenuation gain and $f(a_{k-i})$ is based on the cosine function.

1   41.   The magnetic storage device of claim 40, wherein $f(a_{k-i})$ is chosen to be

2     $a_{k-i}-a_{k-i-2}$, wherein written bits that are to be detected, a_{k-i} , are convolved with a PR4

3   response based upon the cosine function.

1   42.   The magnetic storage device of claim 40, wherein $f(a_{k-i})$ is chosen to be

2      $a_{k-i} + a_{k-i-1} - a_{k-i-2} - a_{k-i-3}$, wherein written bits that are to be detected, a_{k-i} , are convolved

3   with the EPR4 response based upon the cosine function.

1   43.   The magnetic storage device of claim 40, wherein $f(a_{k-i})$ is chosen to be $a_{k-i}t_k$,

2   wherein written bits that are to be detected, a_{k-i} , are convolved with t_k based upon the

3   cosine function.

1   44.   The magnetic storage device of claim 40, wherein $f(a_{k-i})$ is chosen to be $a_{k-i}h_k$,

2   wherein written bits that are to be detected, a_{k-i} , are convolved with h_k based upon the

3   cosine function.

1   45.   A read channel, comprising:

2   means for equalizing a digital signal to provide equalized reproduced signals; and

3   means, coupled to the means for equalizing, for receiving the equalized

4   reproduced signals and converting the reproduced signals into a digital output signal

5   indicative of data stored on a recording medium;

6   wherein the means for equalizing is implemented using means for adaptively

7   updating coefficients for the means for equalizing based upon a cosine function.

1   46. A waveform equalizer that equalizes a waveform of a reproduction signal

2   obtained by reproducing marks and non-marks recorded on a recording medium,

3   comprising:

4   means for delaying propagation of a reproduced signal;

5   means for multiplying predetermined coefficients by the reproduced signal and

6   the delayed signal from the means for delaying;

7   means for adaptively updating the predetermined coefficients for the means for

8   multiplying; and

9   means for adding outputs from the means for multiplying;

10   wherein the means for adaptively updating the predetermined coefficients updates

11   the predetermined coefficients based upon a cosine function.